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(71) Applicant: TRIQUINT SEMICONDUCTOR, INC. [US/US]; 2300 N.E. Brookwood Parkway, Hillsboro, OR 97124 (US).

(72) Inventor: APEL, Thomas, R.; 3144 N.W. Chapin Drive, Portland, OR 97229 (US).

(74) Agents: ALLENBY, Christopher, B. et al.; Skjerven Morrill LLP, 25 Metro Drive, Suite 700, San Jose, CA 95110 (US).

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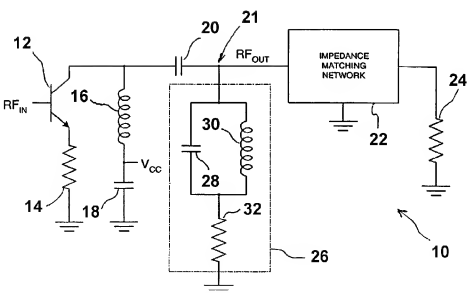
(54) Title: TUNED DAMPING CIRCUIT FOR POWER AMPLIFIER OUTPUT



(57) Abstract: An amplifying circuit (10) includes an amplifying transistor (12) that has a first terminal coupled to receive an input signal (RFIN), a second terminal coupled to a first reference potential, and a third terminal coupled to an output terminal. The amplifying circuit also includes a damping circuit (26) with a first terminal coupled to the output terminal and a second terminal coupled to the first reference potential or a second reference potential. The damping circuit (16) includes a capacitor (28) and inductor (30)coupled in parallel, as well as a resistor (32) coupled in series with the capacitor and the inductor. In one embodiment, the damping circuit (26) is tuned to present a maximum impedance at the operating frequency of the amplifying circuit (10). This reduces or eliminates parametric mode instabilities caused by non-linear capacitive elements on the output side of the amplifying circuit (10).

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TUNED DAMPING CIRCUIT FOR POWER AMPLIFIER OUTPUT

BACKGROUND

1. Field of invention

The present invention relates to amplifiers, and in particular to a tuned damping circuit for power amplifier output.

2. Related art

Radio frequency (RF) power amplifiers are commonly used for signal transmission in wireless communication equipment such as mobile telephones. These power amplifiers typically have one or more amplifier stages using bipolar transistors such as Gallium Arsenide (GaAs) heterojunction bipolar transistors (HBTs). On the output side of such a power amplifier circuit, non-linear capacitive elements can have the undesirable effect of creating parametric mode instabilities, or out-of-band oscillations.

Therefore, a need has arisen for an amplifier that addresses the disadvantages and deficiencies of the prior art. In particular, a need has arisen for an amplifying circuit with a tuned damping circuit to reduce or eliminate parametric mode instabilities.

SUMMARY

An amplifying circuit is disclosed which, in one embodiment, includes an amplifying transistor that has a first terminal coupled to receive an input signal, a second terminal coupled to a first reference potential, and a third terminal coupled to an output terminal. The amplifying circuit also includes a damping circuit with a first terminal coupled to the output terminal and a second terminal coupled to the first reference potential or a

second reference potential. The damping circuit includes a capacitor and inductor coupled in parallel, as well as a resistor coupled in series with the capacitor and the inductor. In one embodiment, the damping circuit is tuned to present a maximum impedance at the operating frequency of the amplifying circuit.

An advantage of the present invention is that parametric mode instabilities, or out-of-band oscillations, caused by non-linear capacitive elements on the output side of the amplifying circuit are reduced or eliminated. Another advantage of the present invention is that this reduction or elimination is achieved with a simple, economical circuit design which has a minimal impact on the amplifying circuit at the amplifying circuit's operating frequency.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and for further features and advantages, reference is now made to the following description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a schematic diagram in partial block form of a power amplifier circuit including a tuned damping circuit;

FIGURE 2 is a graph of reactance as a function of frequency for the damping circuit;

FIGURE 3 is a schematic diagram of a second power amplifier circuit;

FIGURE 4 is a schematic diagram of a third power amplifier circuit; and

FIGURE 5 is a schematic diagram of an exemplary parallel amplifying circuit arrangement.

DETAILED DESCRIPTION

The preferred embodiments of the present invention and their advantages are best understood by referring to FIGURES 1 through 5 of the drawings. Like numerals are used for like and corresponding parts of the various drawings.

FIGURE 1 is a schematic diagram in partial block form of a power amplifier circuit 10 designed in accordance with the present invention. Power amplifier circuit 10 includes an amplifying transistor 12 which may be, for example, a heterojunction bipolar transistor. It will be understood that amplifying transistor 12 may form a single cell in a multi-cell amplifier stage, in which many amplifying transistors like amplifying transistor 12 may be connected in parallel to enhance output power. Amplifying transistor 12 is shown with an emitter ballast resistor 14 connected between the emitter of amplifying transistor 12 and ground.

Conventional circuitry such as a base bias circuit and DC blocking transistor coupling the RF input signal RF_{IN} to the base of amplifying transistor 12 is omitted from FIGURE 1 for simplicity. It will be realized that such conventional circuitry, as well as other known circuitry such as a base ballast resistor in addition to or instead of emitter ballast resistor 14, may also form part of power amplifier circuit 10. An exemplary parallel amplifying arrangement with such conventional circuitry is shown in FIGURE 5.

Returning to FIGURE 1, the collector of amplifying transistor 12 is connected to a supply voltage V_{CC} through an RF choke inductor 16. A large bypass capacitor 18, which acts as a short circuit for RF signals, is connected between inductor 16 and ground.

The collector of amplifying transistor 12 is also connected to a DC blocking capacitor 20, which is in turn connected to an output node 21. An RF output signal RF_{OUT} is

provided at output node 21. Output node 21 is coupled to a load resistance 24 through an impedance matching network 22, which may be of conventional design.

A damping circuit 26 is connected to output node 21. Damping circuit 26 is a tuned damping circuit designed to damp out-of-band oscillations. Damping circuit 26 includes a capacitor 28 and an inductor 30 connected to output node 21 in parallel. The parallel arrangement of capacitor 28 and inductor 30 is connected in series with a resistor 32, which is connected to ground. Of course, damping circuit 26 may be inverted, so that resistor 32 is connected to output node 21 and capacitor 28 and inductor 30 are connected to ground. In this alternative arrangement, damping circuit 26 still performs its function as described below.

Damping circuit 26 is tuned to present a maximum impedance in the operating frequency range of power amplifier circuit 10, and a very low impedance out-of-band. Referring to FIGURE 2, a graph of the reactance X of damping circuit 26 as a function of frequency is shown. In this graph, the operating frequency range is defined by dashed lines 34, with a central operating frequency illustrated by dashed line 36. As shown in the graph, damping circuit 26 has a high reactance with the operating frequency range. Above the central operating frequency, the reactance is capacitive. Below the central operating frequency, the reactance is inductive. In either case, resistor 32 provides a load for out-of-band frequencies, but is not significant within the operating frequency range compared with the reactance of capacitor 28 and inductor 30. In this manner, out-of-band oscillations are damped, while the operating frequency range is substantially unaffected.

For purposes of illustration, exemplary values for the components and operation of power amplifier circuit 10 are presented in Table A.

TABLE A

Operating Frequency Range:		1900 MHz
Resistors:	14	0.1 Ohm
	24	50 Ohm
	32	5 Ohm
Capacitors:	18	100 pF
	20	20 pF
	28	2.1 pF
Inductors:	16	10.0 nH
	30	3.3 nH

Referring to FIGURE 3, a schematic diagram of an alternative power amplifier circuit 40 is shown. Power amplifier circuit 40 is similar to power amplifier circuit 10 described above, and like numerals are used for like and corresponding parts of FIGURES 1 and 3.

In power amplifier circuit 40, damping circuit 26 is connected in parallel with RF choke inductor 16. Thus, rather than being DC connected to ground, resistor 32 is DC connected to V_{cc} and RF coupled to ground through capacitor 18. The only other difference between circuits 10 and 40 is the placement of DC blocking capacitor 20 relative to damping circuit 26, which is purely a matter of design choice and has no significant impact on the operational characteristics of the circuit.

Damping circuit 26 performs the same function in power amplifier circuit 40 as in power amplifier circuit 10, which is to damp out-of-band oscillations. Thus, the two circuits 10 and 40 operate in a substantially identical manner.

Referring to FIGURE 4, a schematic diagram of a third power amplifier circuit 50 is shown. Power amplifier circuit 50 has a stabilizing circuit 52 in series (rather than in shunt) with the output signal path. The stabilizing

circuit 52 consists of a resistor 54 in parallel with a series arrangement of an inductor 56 and a capacitor 58.

It will be appreciated that power amplifier circuit 50 is equivalent to power amplifier circuit 10 in terms of impedance characteristics. Thus, power amplifier circuit 50 exhibits the same out-of-band stability as power amplifier circuits 10 and 40.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the invention as defined by the following claims.

CLAIMS

I claim:

1. An amplifying circuit comprising:

an amplifying transistor having a first terminal coupled to receive an input signal, the amplifying transistor having a second terminal coupled to a first reference potential, the amplifying transistor having a third terminal coupled to an output terminal; and

a damping circuit having a first terminal coupled to the output terminal and having a second terminal coupled to a selected one of the first reference potential and a second reference potential, the damping circuit further having a capacitor, an inductor coupled in parallel with the capacitor, and a resistor coupled in series with the capacitor and the inductor.

2. The amplifying circuit of claim 1, wherein:

the capacitor of the damping circuit has a first terminal connected to the first terminal of the damping circuit;

the inductor of the damping circuit has a first terminal connected to the first terminal of the damping circuit, the inductor further having a second terminal connected to a second terminal of the capacitor; and

the resistor of the damping circuit has a first terminal connected to the second terminal of the capacitor, the resistor further having a second terminal connected to the second terminal of the damping circuit.

3. The amplifying circuit of claim 1, wherein the first terminal of the damping circuit is connected to the output terminal, and wherein the second terminal of the damping circuit is connected to ground.

4. The amplifying circuit of claim 3, further comprising an RF choke inductor coupled between the output terminal and a voltage supply terminal.

5. The amplifying circuit of claim 1, wherein the first terminal of the damping circuit is connected to the output terminal, and wherein the second terminal of the damping circuit is connected to a voltage supply terminal.

6. The amplifying circuit of claim 5, further comprising an RF choke inductor coupled between the output terminal and a voltage supply terminal.

7. The amplifying circuit of claim 1, wherein the damping circuit is tuned to present a maximum impedance at an operating frequency of the amplifying circuit.

8. The amplifying circuit of claim 1, wherein the first reference potential comprises a ground potential.

9. The amplifying circuit of claim 8, wherein the second reference potential comprises a voltage supply potential.

10. The amplifying circuit of claim 1, further comprising an impedance matching network coupled to the output terminal.

11. The amplifying circuit of claim 1, further comprising a ballast resistor connected between the first reference potential and the second terminal of the amplifying transistor.

12. The amplifying circuit of claim 1, wherein the amplifying transistor comprises a bipolar transistor, and wherein the first terminal of the amplifying transistor

comprises a base terminal, and wherein the second terminal of the amplifying transistor comprises an emitter terminal, and wherein the third terminal of the amplifying transistor comprises a collector terminal.

13. The amplifying circuit of claim 1, wherein the amplifying transistor comprises a heterojunction bipolar transistor

14. An amplifying circuit comprising:

an amplifying transistor having a first terminal coupled to receive an input signal, the amplifying transistor having a second terminal coupled to a reference potential; and

a damping circuit having a first terminal coupled to a third terminal of the amplifying transistor, the damping circuit having a second terminal coupled to an output terminal of the amplifying circuit, the damping circuit further having a capacitor, an inductor coupled in series with the capacitor, and a resistor coupled in parallel with the capacitor and the inductor.

15. The amplifying circuit of claim 14, wherein:

the capacitor of the damping circuit has a first terminal connected to the second terminal of the damping circuit;

the inductor of the damping circuit has a first terminal connected to the first terminal of the damping circuit, the inductor further having a second terminal connected to a second terminal of the capacitor; and

the resistor of the damping circuit has a first terminal connected to the first terminal of the damping circuit, and a second terminal connected to the second terminal of the damping circuit.

16. The amplifying circuit of claim 14, further comprising:

an RF choke inductor coupled between the third terminal of the amplifying transistor and a voltage supply terminal; and

a second capacitor coupled between the voltage supply terminal and the reference potential.

17. An amplifying circuit comprising:

a bias circuit operable to generate a bias voltage at a bias voltage terminal;

a plurality of amplifying transistors each having a first terminal coupled to the bias voltage terminal, a second terminal coupled to a first reference potential, and a third terminal coupled to a common output terminal, the first terminal being coupled to receive an input signal; and

a damping circuit having a first terminal coupled to the common output terminal and having a second terminal coupled to a selected one of the first reference potential and a second reference potential, the damping circuit further having a capacitor, an inductor coupled in parallel with the capacitor, and a resistor coupled in series with the capacitor and the inductor.

18. The amplifying circuit of claim 17, further comprising a plurality of DC blocking capacitors, each DC blocking capacitor having a first terminal connected to an input signal source and a second terminal connected to the first terminal of a corresponding one of the amplifying transistors.

19. The amplifying circuit of claim 17, wherein each amplifying transistor comprises a bipolar transistor, and wherein the first terminal of each amplifying transistor

comprises a base terminal, and wherein the second terminal of each amplifying transistor comprises an emitter terminal, and wherein the third terminal of each amplifying transistor comprises a collector terminal.

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20. The amplifying circuit of claim 17, wherein at least one of the amplifying transistors comprises a heterojunction bipolar transistor.

10 21. The amplifying circuit of claim 17, wherein the damping circuit is tuned to present a maximum impedance at an operating frequency of the amplifying circuit.

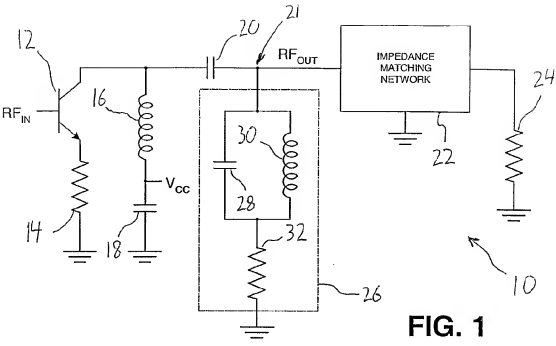
12
20
21
RF_OUT
IMPEDANCE MATCHING NETWORK
24
RF_IN
16
30
22
V_CC
28
14
18
32
26
10

FIG. 1

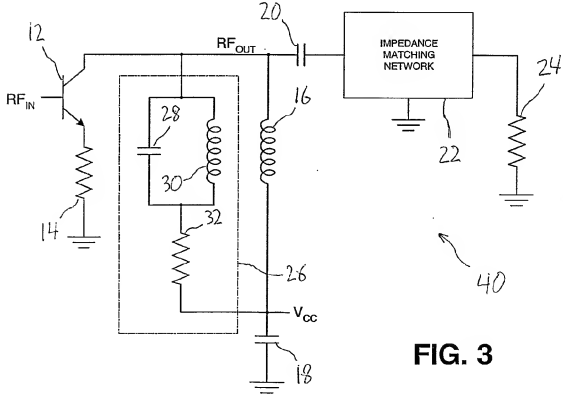
20
12
RF_OUT
IMPEDANCE MATCHING NETWORK
24
RF_IN
28
16
22
30
32
14
26
40
V_CC
18

FIG. 3

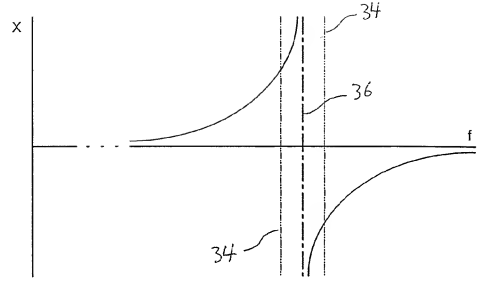

FIG. 2

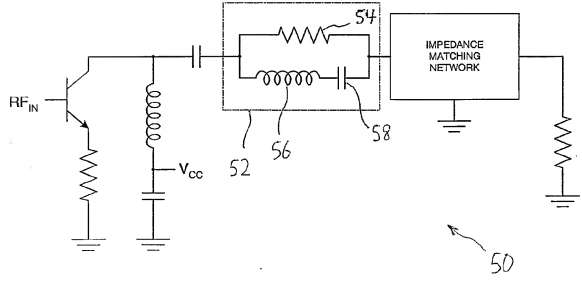

FIG. 4

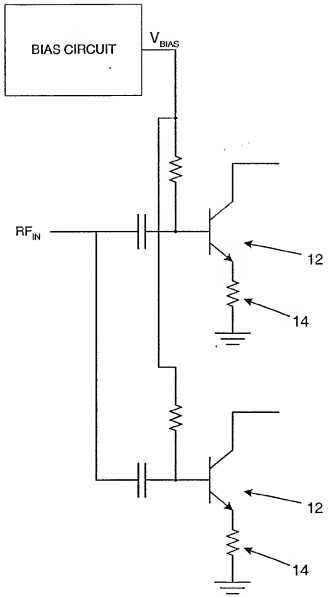

FIG. 5